sea of N memory cells to N/k x k bits, where k is a power of two.

2 ~~13~~. The field programmable memory cell array of Claim 1 ~~12~~, wherein said programmable address decoder comprises a plurality of mode control lines respectively connected to control inputs of a plurality of paired demultiplexers, with one data input of each of said paired demultiplexers being respectively connected to four column address lines and the other data input of each of said paired demultiplexers being respectively connected to the complement of said column address lines and with outputs of said demultiplexers being logically connected to enable inputs of the column decoder such that k columns of the memory cells are addressed thereby defining a word width of k bits wide.

3 ~~14~~. The field programmable memory cell array of Claim 2 ~~13~~, wherein said programmable interconnect comprises a plurality of switches, controlled by said mode control lines, connected between respective data lines of the input/output circuits to yield a word width of k bits wide.

4 ~~15~~. The field programmable memory cell array of Claim 3 ~~14~~, wherein said switches comprise PASS transistors.

5 ~~16~~. The field programmable memory cell array of Claim 1 ~~12~~, wherein said programmable interconnect comprises a plurality of switches, controlled by a plurality of mode control lines, connected between respective data lines of the input/output circuits to yield a word width of k bits wide.

6 ~~17~~. The field programmable memory cell array of Claim 5 ~~16~~,

wherein said switches comprise PASS transistors.

~~18~~ 7. The field programmable memory cell array of Claim ~~16~~ 5, wherein said programmable address decoder comprises a plurality of paired demultiplexers, with said mode control lines respectively connected to control inputs thereof, with one data input of each of said paired demultiplexers being respectively connected to four column address lines and the other data input of each of said paired demultiplexers being respectively connected to the complement of said column address lines and with outputs of said demultiplexers being logically connected to enable inputs of the column decoder such that k columns of the memory cells are addressed thereby defining a word width of k bits wide.

~~19~~ 8. A method for programming a field programmable memory cell array including a memory array composed of a sea of N memory cells addressed by a row decoder and a column decoder to input or output data by means of input/output circuits, input data control circuits and output data control circuits as determined by select/write enable logic, comprising the steps of programming an address decoder and an interconnect to selectively reconfigure the sea of N memory cells to N/k x k bits, where k is a power of two.

~~20~~ 9. The programming method of Claim ~~19~~ 8, wherein the step of programming the address decoder comprises the steps of addressing enable inputs of the column decoder such that k columns of the

memory cells are addressed thereby defining a word width of k bits wide.

Cl cond D 10 ~~21~~. The programming method of Claim 9 ~~20~~, wherein the step of programming the interconnect comprises the step of programming a plurality of switches connected between respective data lines of the input/output circuits to yield a word width of k bits wide.

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